EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"6,668,304".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L2	5000	write adj transaction$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L3	284057	tag$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L4	81	L2 near5 L3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L5	72	L4 and @ad<"20040227"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L6	68	L5 and 7$2/$3.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L7	160	L2 with L3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56

EAST Search History

L8	4131	tag$1 near2 generat$3	USPAT; USOCR	OR	OFF	2007/10/17 13:56
L9	66	L7 and @ad<"20040227" and "711"/$3.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L10	3	L8 and L9	USPAT; USOCR	OR	OFF	2007/10/17 13:56
L11	42	write adj transaction$1 same tag$1 same generat$3 and (virtual logical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L12	66	write adj transaction$1 with tag$1 and "711"/$3.ccls. and @ad<"20040227"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L13	14	write adj transaction$1 same tag$1 and tag$1 near3 generat$3 and (virtual logical) and "711"/$3.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L14	2	"7080198".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L15	1152	711/203.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56

EAST Search History

L16	1	L15 and (L2 same L3) and @ad<"20040227"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L17	1	write adj transaction$1 with (field$1 tag$1 header$1) near3 (includ$3 compris$3) same (relat$3 link$3) and "711"/$3.ccls. and @ad<"20040227"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L18	1	"6418494".PN.	USPAT; USOCR	OR	OFF	2007/10/17 13:56
L19	1	"6389526".PN.	USPAT; USOCR	OR	OFF	2007/10/17 13:56
L20	1	"6557048".PN.	USPAT; USOCR	OR	OFF	2007/10/17 13:56
L21	1	"6385705".PN.	USPAT; USOCR	OR	OFF	2007/10/17 13:56
L22	12793	mirror$3 same (virtual logical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L23	1	L6 and L22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L24	1	L15 and L12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L25	0	write adj transaction$1 with (field$1 tag$1 header$1) with (includ$3 compris$3) and (cop$4 mirror$3) same (logical virtual) and "711"/$3. ccls. and @ad<"20040227"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56

EAST Search History

L26	0	"write transaction" same tag$1 same (virtual logical) same mirror$3	USPAT; USOCR	OR	OFF	2007/10/17 13:56
L27	937	(karr.in. jonnala.in. valiveti.in. joshi.in.)	US-PGPUB	OR	OFF	2007/10/17 13:56
L28	351	370/355.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L29	937	370/356.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L30	2084	709/245.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L31	4139	709/227.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L32	2136	709/228.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L33	0	L27 and "write transactions".clm.	US-PGPUB	OR	OFF	2007/10/17 13:56
L34	885	711/207.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56

EAST Search History

L35	228	711/208.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L36	2151	709/231.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L37	1045	709/236.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L38	3	"6,834,326".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L39	0	"write transaction" same tag$1 same (virtual logical) and mirror$3 same (virtual logical)	USPAT; USOCR	OR	OFF	2007/10/17 13:56
L40	36	write adj transaction$1 with (field$1 tag$1 header$1) with (includ$3 compris$3) and "711"/$3.ccls. and @ad<"20040227"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L41	10	write adj transaction$1 with tag$1 and tag$1 near3 generat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L42	0	L27 and (write adj transactions).clm.	US-PGPUB	OR	OFF	2007/10/17 13:56

EAST Search History

L43	0	write adj transaction$1 same tag$1 same generat$3 and mirror$3 same (virtual logical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L44	0	write adj transaction$1 same tag$1 same generat$3 and mirror$3 same (virtual logical)	USPAT; USOCR	OR	OFF	2007/10/17 13:56
L45	160	write adj transaction$1 with tag$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L46	130	L7 and @ad<"20040227" and 7$2/$3. ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L47	609	711/200.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L48	309	711/205.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L49	1009	711/206.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56

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L50	10	write adj transaction$1 with tag$1 near3 (includ$3 compris$3) and "711"/$3.ccls. and @ad<"20040227"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L51	3793606	@ad<"20040227"	USPAT; USOCR	OR	OFF	2007/10/17 13:56
L52	3	L51 and mirrored adj (transaction write) same (tag ID identifier label) with (data blocks stripes)	USPAT; USOCR	OR	ON	2007/10/17 13:56
L53	1	L51 and mirrored adj (transaction write) same (tag ID identifier label) with (identical "same") same (data blocks stripes)	USPAT; USOCR	OR	ON	2007/10/17 13:56
L54	3	L51 and mirrored adj (transaction write) with (tag ID identifier label)	USPAT; USOCR	OR	ON	2007/10/17 13:56
L55	13	L51 and mirrored adj (transaction write) same (tag ID identifier label)	USPAT; USOCR	OR	ON	2007/10/17 13:56
L56	158	L51 and mirror$3 with (transaction write) same (tag$4 ID identi$5 label$3) with (identical "same" equivalent)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L57	13	L51 and mirrored adj (transaction write) same (tag ID identifier label)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L58	5	L51 and mirror$3 near2 (transaction write) same (tag$4 ID identi$5 label$3) near3 (identical "same" equivalent)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L59	60	L51 and mirror$3 near2 (transaction write) and (tag$4 ID identi$5 label$3) with (table TLB) same (logical virtual)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56

EAST Search History

L60	31	L51 and mirror$3 near2 (transaction write) and (tag$4 ID identi$5 label$3) with (stor$3 sav$3 retain$3) with (table TLB) same (logical virtual)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L61	86	L51 and (mirror$3 duplicat$3 cop$4) same (tag$4 ID identifier label$3 pointer) with table same (logical virtual) and entr$3 with match$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L62	33	L51 and (mirror$3 duplicat$3 cop$4) same (tag$4 ID identifier label$3 pointer) with table same (logical virtual) same entr$3 with match$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L63	89	L51 and tag$4 with table same (logical virtual) same entr$3 with match$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L64	23	L51 and tag$4 near3 table same (logical virtual) same entr$3 near5 match$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L65	0	L51 and mirror$3 near2 (transaction write) same (tag$4 ID identi$5 label$3) with (table TLB) same (logical virtual)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 14:59
L66	7	L51 and mirror$3 near2 (transaction write) and (tag$4 ID identifier label$3) with (stor$3 sav$3 retain$3) with (table TLB) same (logical virtual)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56

EAST Search History

L67	6	("6029166" | "6038639" | "6058054" | "6078932" | "6161111" | "6212531").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/10/17 13:56
L68	97	L51 and mirror$3 and (tag$4 ID identifier label$3) with (stor$3 sav$3 retain$3) with (table TLB) same (logical virtual)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L69	25	L51 and mirror$3 and (tag$4 ID identifier$1 label$3) with (stor$3 sav$3 retain$3) with (table TLB) same (logical virtual) same tables	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L70	21	L51 and mirror$3 same (tag$4 ID identifier label$3 pointer) with (stor$3 sav$3 retain$3) with (table TLB) same (logical virtual)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L71	0	L51 and mirror$3 same "tag tables"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L72	1	L51 and mirror$3 same tag adj table$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L73	159	L51 and mirror$3 and (tag$4 ID identifier label$3 pointer) with (stor$3 sav$3 retain$3) with (table TLB) same (logical virtual)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L74	13	("6804755").URPN.	USPAT	OR	ON	2007/10/17 13:56
L75	6	("6029166" | "6038639" | "6058054" | "6078932" | "6161111" | "6212531").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/10/17 13:56

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L76	84	L51 and (mirror$3 duplicat$3 cop$4) same (tag$4 ID identifier label$3 pointer) with (table TLB) same (logical virtual) same object	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L77	18	L51 and (mirror$3 duplicat$3 cop$4) same (tag$4 ID identifier label$3 pointer) with table with (separate different) same (logical virtual)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L78	3	L51 and (mirror$3 duplicat$3 cop$4) same (tag$4 ID identifier label$3 pointer) with table with (separate different) same (logical virtual) same object	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 13:56
L79	2	"6,804,755".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L80	2	"5,787,485".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 13:56
L81	1054364	(synchroniz$6 resynchroniz$6 updat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 14:56
L82	2190841	(match$3 duplicat$3 copy copies version)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 14:59

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L84	653	51 and (tag$4 ID identi$5 label$3) with (table TLB) same (logical virtual) and (table TLB) with 81 same 82	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 15:08
L85	230	51 and (tag$4 ID identi$5 label$3) near3 (table TLB) same (logical virtual) and (table TLB) near3 81 same 82	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 15:02
L86	139	51 and (tag$4 ID identi$5 label$3) near3 (table TLB) same (logical virtual) and (table TLB) near3 81 same match$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/17 15:02
L87	155	51 and (tag$4 ID identi$5 label$3) with (tables TLB$1) same (logical virtual) and (tables TLB$1) with 81 same 82	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/10/17 15:09

Terms used:
write transactions tags entries device tables synchronizing virtual logical

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Relevance scale

1 Essays in computing science

C. A. R. Hoare
January 1989 Book

Publisher: Prentice-Hall, Inc.

Full text available: pdf(20.91 MB) Additional Information: full citation, abstract, references, cited by, review

Charles Antony Richard Hoare is one of the most productive and prolific computer scientists. This volume contains a selection of his published papers. There is a need, as in a Shakespearian Chorus, to offer some apology for what the book manifestly fails to achieve. It is not a complete 'collected works'. Selection between papers of this quality is not easy and, given the book's already considerable size, some difficult decisions as to what to omit have had to be made. Pity the editor weighin ...

2 Cryptography and data security

Dorothy Elizabeth Robling Denning
January 1982 Book

Publisher: Addison-Wesley Longman Publishing Co., Inc.

Full text available: pdf(19.47 MB) Additional Information: full citation, abstract, references, cited by, index terms

From the Preface (See Front Matter for full Preface)

Electronic computers have evolved from exiguous experimental enterprises in the 1940s to prolific practical data processing systems in the 1980s. As we have come to rely on these systems to process and store data, we have also come to wonder about their ability to protect valuable data.

Data security is the science and study of methods of protecting data in computer and communication systems from unauthorized disclosure ...

3 The multics system: an examination of its structure

Elliott I. Organick
January 1972 Book

Publisher: MIT Press

Additional Information: full citation, abstract, references, cited by, index terms

This volume provides an overview of the Multics system developed at M.I.T.--a time-

shared, general purpose utility like system with third-generation software. The advantage that this new system has over its predecessors lies in its expanded capacity to manipulate and file information on several levels and to police and control access to data in its various files. On the invitation of M.I.T.'s Project MAC, Elliott Organick developed over a period of years an explanation of the workings, concep ...

4 GPGPU: general purpose computation on graphics hardware

David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(63.03 MB) Additional Information: full citation, abstract, citings

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flexible processor. The latest graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully programmable vertex and pixel processing units that support vector operations up to full IEEE floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

5 Real-time shading

Marc Olano, Kurt Akeley, John C. Hart, Wolfgang Heidrich, Michael McCool, Jason L. Mitchell, Randi Rost

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(7.39 MB) Additional Information: full citation, abstract

Real-time procedural shading was once seen as a distant dream. When the first version of this course was offered four years ago, real-time shading was possible, but only with one-of-a-kind hardware or by combining the effects of tens to hundreds of rendering passes. Today, almost every new computer comes with graphics hardware capable of interactively executing shaders of thousands to tens of thousands of instructions. This course has been redesigned to address today's real-time shading capabili ...

6 A structural view of the Cedar programming environment

Daniel C. Swinehart, Polle T. Zellweger, Richard J. Beach, Robert B. Hagmann

August 1986 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 8 Issue 4

Publisher: ACM Press

Full text available: pdf(6.32 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

7 Logged virtual memory

D. R. Cheriton, K. J. Duda

December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles SOSP '95**, Volume 29 Issue 5

Publisher: ACM Press

Full text available: pdf(1.52 MB) Additional Information: full citation, references, citings, index terms

8 System support for pervasive applications

Robert Grimm, Janet Davis, Eric Lemar, Adam Macbeth, Steven Swanson, Thomas Anderson, Brian Bershad, Gaetano Borriello, Steven Gribble, David Wetherall
November 2004 **ACM Transactions on Computer Systems (TOCS)**, Volume 22 Issue 4
Publisher: ACM Press

Full text available: pdf(1.82 MB) Additional Information: full citation, abstract, references, citings, index terms

Pervasive computing provides an attractive vision for the future of computing. Computational power will be available everywhere. Mobile and stationary devices will dynamically connect and coordinate to seamlessly help people in accomplishing their tasks. For this vision to become a reality, developers must build applications that constantly adapt to a highly dynamic computing environment. To make the developers' task feasible, we present a system architecture for pervasive computing, called & ...

Keywords: Asynchronous events, checkpointing, discovery, logic/operation pattern, migration, one.world, pervasive computing, structured I/O, tuples, ubiquitous computing

9 Anatomy of a native XML base management system

T. Fiebig, S. Helmer, C.-C. Kanne, G. Moerkotte, J. Neumann, R. Schiele, T. Westmann
December 2002 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 11 Issue 4
Publisher: Springer-Verlag New York, Inc.
Full text available: pdf(300.97 KB) Additional Information: full citation, abstract, citings, index terms

Several alternatives to manage large XML document collections exist, ranging from file systems over relational or other database systems to specifically tailored XML base management systems. In this paper we give a tour of Natix, a database management system designed from scratch for storing and processing XML data. Contrary to the common belief that management of XML data is just another application for traditional databases like relational systems, we illustrate how almost every component in a ...

Keywords: Database, XML

10 Software-controlled caches in the VMP multiprocessor

D. R. Cheriton, G. A. Slavenburg, P. D. Boyle
June 1986 **ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture ISCA '86**, Volume 14 Issue 2
Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(958.63 KB) Additional Information: full citation, abstract, references, citings, index terms

VMP is an experimental multiprocessor that follows the familiar basic design of multiple processors, each with a cache, connected by a shared bus to global memory. Each processor has a synchronous, virtually addressed, single master connection to its cache, providing very high memory bandwidth. An unusually large cache page size and fast sequential memory copy hardware make it feasible for cache misses to be handled in software, analogously to the handling of virtual memory page faults. Har ...

11 Link and channel measurement: A simple mechanism for capturing and replaying wireless channels

Glenn Judd, Peter Steenkiste

August 2005 **Proceeding of the 2005 ACM SIGCOMM workshop on Experimental approaches to wireless network design and analysis E-WIND '05**

Publisher: ACM Press

Full text available: pdf(6.06 MB) Additional Information: full citation, abstract, references, index terms

Physical layer wireless network emulation has the potential to be a powerful experimental tool. An important challenge in physical emulation, and traditional simulation, is to accurately model the wireless channel. In this paper we examine the possibility of using on-card signal strength measurements to capture wireless channel traces. A key advantage of this approach is the simplicity and ubiquity with which these measurements can be obtained since virtually all wireless devices provide the req ...

Keywords: channel capture, emulation, wireless

12 Compiler construction: an advanced course

F. L. Bauer, F. L. De Remer, M. Griffiths, U. Hill, J. J. Horning, C. H. A. Koster, W. M. McKeeman, P. C. Poole, W. M. Waite, G. Goos, J. Hartmanis

January 1974 Book

Publisher: Springer-Verlag New York, Inc.

Additional Information: full citation, abstract, references, cited by

The Advanced Course took place from March 4 to 15, 1974 and was organized by the Mathematical Institute of the Technical University of Munich and the Leibniz Computing Center of the Bavarian Academy of Sciences, in co-operation with the European Communities, sponsored by the Ministry for Research and Technology of the Federal Republic of Germany and by the European Research Office, London.

13 Decoupled hardware support for distributed shared memory

Steven K. Reinhardt, Robert W. Pfile, David A. Wood

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2

Publisher: ACM Press

Full text available: pdf(1.47 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper investigates hardware support for fine-grain distributed shared memory (DSM) in networks of workstations. To reduce design time and implementation cost relative to dedicated DSM systems, we decouple the functional hardware components of DSM support, allowing greater use of off-the-shelf devices.We present two decoupled systems, Typhoon-0 and Typhoon-1. Typhoon-0 uses an off-the-shelf protocol processor and network interface; a custom access control device is the only DSM-specific hard ...

14 Fault Tolerant Operating Systems

Peter J. Denning

December 1976 **ACM Computing Surveys (CSUR)**, Volume 8 Issue 4

Publisher: ACM Press

Full text available: pdf(2.69 MB) Additional Information: full citation, references, citings, index terms

15 Logical and physical design issues for smart card databases

Cristiana Bolchini, Fabio Salice, Fabio A. Schreiber, Letizia Tanca

July 2003 **ACM Transactions on Information Systems (TOIS)**, Volume 21 Issue 3

Publisher: ACM Press

Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, citings, index terms

The design of very small databases for smart cards and for portable embedded systems is deeply constrained by the peculiar features of the physical medium. We propose a joint approach to the logical and physical database design phases and evaluate several data structures with respect to the performance, power consumption, and endurance parameters of read/program operations on the Flash-EEPROM storage medium.

Keywords: Design methodology, access methods, data structures, flash memory, personal information systems, smart card

16 The apprentice challenge

J. Strother Moore, George Porter

May 2002 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 24 Issue 3

Publisher: ACM Press

Full text available: pdf(212.09 KB) Additional Information: full citation, abstract, references, citings, index terms

We describe a mechanically checked proof of a property of a small system of Java programs involving an unbounded number of threads and synchronization, via monitors. We adopt the output of the javac compiler as the semantics and verify the system at the bytecode level under an operational semantics for the JVM. We assume a sequentially consistent memory model and atomicity at the bytecode level. Our operational semantics is expressed in ACL2, a Lisp-based logic of recursive functions. Our proofs ...

Keywords: Java, Java Virtual Machine, mutual exclusion, operational semantics, parallel and distributed computation, theorem proving

17 Tempest and typhoon: user-level shared memory

S. K. Reinhardt, J. R. Larus, D. A. Wood

April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture ISCA '94**, Volume 22 Issue 2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references, citings, index terms

Future parallel computers must efficiently execute not only hand-coded applications but also programs written in high-level, parallel programming languages. Today's machines limit these programs to a single communication paradigm, either message-passing or shared-memory, which results in uneven performance. This paper addresses this problem by defining an interface, *Tempest*, that exposes low-level communication and memory-system mechanisms so programmers and compilers can customize polici ...

18 An in-cache address translation mechanism

D. A. Wood, S. J. Eggers, G. Gibson, M. D. Hill, J. M. Pendleton

June 1986 **ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture ISCA '86**, Volume 14 Issue 2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(770.30 KB) Additional Information: full citation, abstract, references, citings, index terms

In the design of SPUR, a high-performance multiprocessor workstation, the use of large

caches and hardware-supported cache consistency suggests a new approach to virtual address translation. By performing translation in each processor's virtually-tagged cache, the need for separate translation lookaside buffers (TLBs) is eliminated. Eliminating the TLB substantially reduces the hardware cost and complexity of the translation mechanism and eliminates the translation consistency problem. Trac ...

19 Trace-driven memory simulation: a survey

Richard A. Uhlig, Trevor N. Mudge
June 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 2
Publisher: ACM Press

Full text available: pdf(636.11 KB) Additional Information: full citation, abstract, references, citings, index terms, review

As the gap between processor and memory speeds continues to widen, methods for evaluating memory system designs before they are implemented in hardware are becoming increasingly important. One such method, trace-driven memory simulation, has been the subject of intense interest among researchers and has, as a result, enjoyed rapid development and substantial improvements during the past decade. This article surveys and analyzes these developments by establishing criteria for evaluating trac ...

Keywords: TLBs, caches, memory management, memory simulation, trace-driven simulation

20 Technical reports

SIGACT News Staff
January 1980 **ACM SIGACT News**, Volume 12 Issue 1
Publisher: ACM Press
Full text available: pdf(5.28 MB) Additional Information: full citation

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